

1 An Input/Output Circuit With User Programmable Functions

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7 ABSTRACT OF THE DISCLOSURE

8 The I/O circuit of the present invention provides
9 optimal flexibility and performance using a number of
10 different structures and methods. The present invention
11 provides a signal follower circuit for an input pad. In
12 one embodiment, the output buffer is capable of injecting a
13 constant onto a pad during reconfiguration of a
14 configurable system logic circuit. The present invention
15 also provides a circuit for generating a programmable data
16 propagation delay, thereby guaranteeing zero hold time for
17 an arbitrary input register. Zero hold time is
18 accomplished by allowing the user to optimally characterize
19 clock delay to a given input/output circuit. The present
20 invention also provides fast switching between input pads,
21 thereby minimizing data propagation delay between the input
22 pads. Additionally, the present invention reduces time
23 spent in production product test by facilitating the
24 testing of multiple routes with one test configuration. A
25 circuit expanding the number of data input channels
26 available to system routing is provided. Lastly, a
27 plurality of identical input/output block tiles (IOBTs) is
28 disclosed, thereby enabling each I/O circuit to provide the
29 same signals regardless of the IOBTs location in the I/O
30 circuit.